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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,686	05/26/2006	Katsuhide Uchino	SON-3161	4362

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EXAMINER	
LEWIS, DAVID LEE	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
03/19/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,686	UCHINO ET AL.	
	Examiner	Art Unit	
	DAVID L. LEWIS	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,9,12,16,19,21 and 23* is/are rejected.

7)☒ Claim(s) *2-4,6-8,10,11,13-15,17,18,20,22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/11/2008 (2); 5/26/2006;*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1, 5, 9, 12, 16, 19, 21, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Koyama (6809482).**

As in claims 1 and 19, Koyama teaches of a transistor circuit and method having a plurality of thin-film transistors formed on a substrate and wiring adapted to connect a gate, a source, and/or a drain of each of the thin-film transistors, so as to perform a predetermined operation, **figures 2 and 3, column 5 lines 53-67**,

the transistor circuit comprising: at least one thin-film transistor applied with a forward bias between a gate and a source repeatedly and/or continuously via wiring during the operation, **figure 3 item 106, column 6 lines 1-55**,

and reverse-bias-application means configured to suppress a variation in a threshold voltage of the thin-film transistor by applying a reverse bias between the gate and source of the thin-film transistor in such timing that the operation is not disturbed, **figure 3 item 107, column 6 lines 1-55**.

As in claims 5, 12, 21, and 23, Koyama teaches of a display device and method comprising scan lines in rows, scan lines in columns, and pixel circuits provided at intersections of the scan lines, **figure 1 items 103a/b, figure 3 items Gj, Si, Cj, column 6 lines 1-55**,

wherein, upon being selected by the scan line, the pixel circuit samples a video signal from the signal line and drives a light-emission element according to the sampled video
signal, **figure 1 items 103a/b, figure 3 items Gj, Si, Cj, column 6 lines 1-55,**

and wherein the pixel circuit includes a plurality of thin-film transistors formed on a substrate and wiring adapted to connect a gate, a source, and/or a drain of each of the thin-film transistors, **column 5 lines 29-66, figure 5,**

at least one thin-film transistor applied with a forward bias between a gate and a source repeatedly and/or continuously via wiring while the light-emission element is driven, **figure 3 item 106, column 6 lines 1-55**

and reverse-bias-application means configured to suppress a variation in a threshold voltage of the thin-film transistor by applying a reverse bias between the gate and source of the thin-film transistor in such timing that the driven light-emission element is not disturbed, **figure 3 item 107, column 6 lines 1-55**.

As in claims 9 or 16, Koyama teaches of wherein the plurality of thin-film transistors includes a sampling thin-film transistor that is brought into conduction upon being selected by the scan line, and that samples a signal from the signal line and holds the sampled signal in a holding capacitor, **figure 3 item 105**, a drive thin-film transistor which controls the amount of power applied to the load element according to the potential of the signal held in the holding capacitor, **figure 3 item 106**, and a switching thin-film transistor which performs on/off

control of the amount of power applied to the load element, wherein the reverse-bias-application means applies the reverse bias to at least one of the drive thin-film transistor and the switching thin-film transistor, **figure 3 item 107**.

Claim Objections

2. Claims 2-4, 6-8, 10, 11, 13-15, 17, 18, 20, 22, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis

March 16, 2009

/David L Lewis/

Examiner, Art Unit 2629